FIG. 1

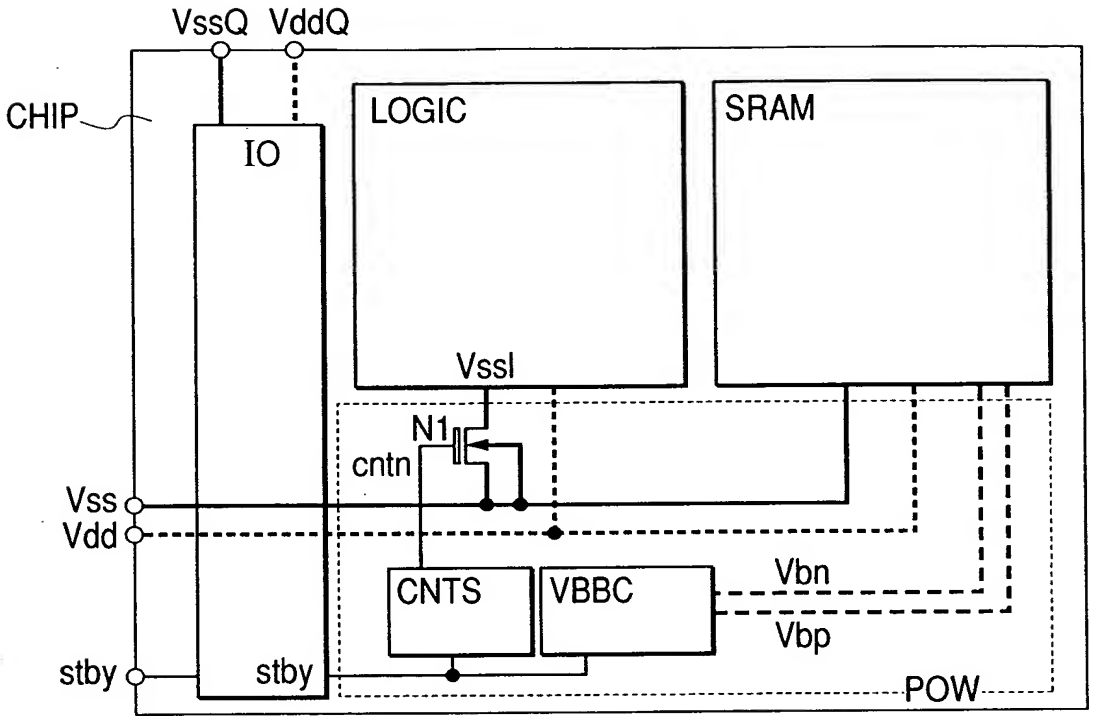

VssQ
VddQ
CHIP
IO
LOGIC
SRAM
Vssl
N1
cntn
Vss
Vdd
CNTS
VBBC
Vbn
Vbp
stby
stby
POW

FIG. 2

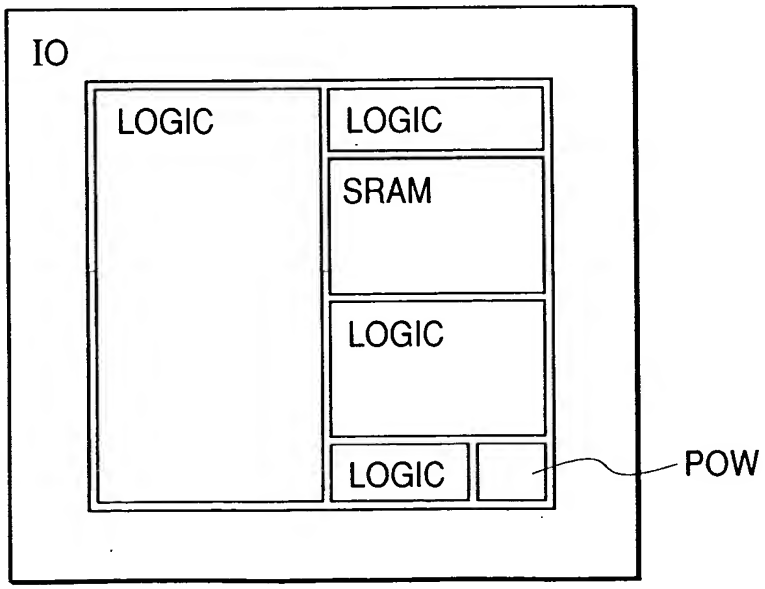

IO
LOGIC
LOGIC
SRAM
LOGIC
LOGIC
POW

FIG. 3

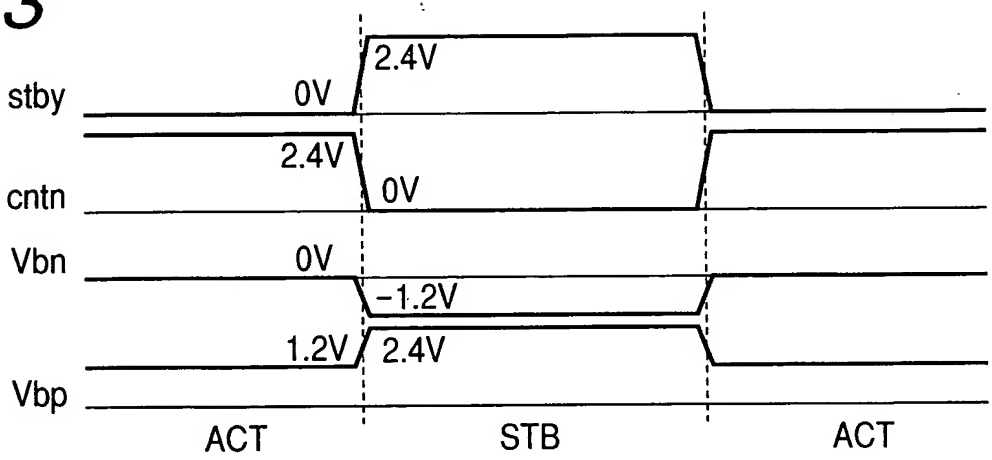


FIG. 4

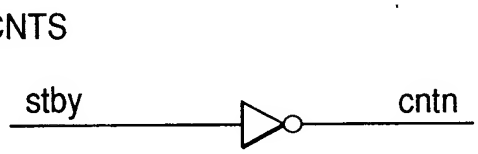


FIG. 5

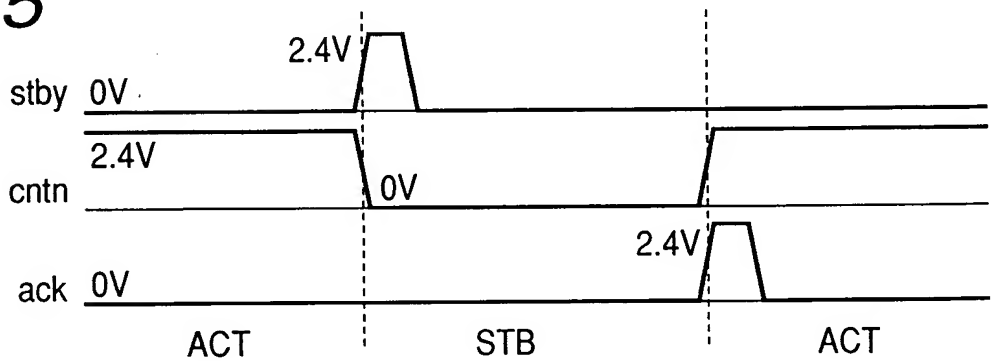


FIG. 6

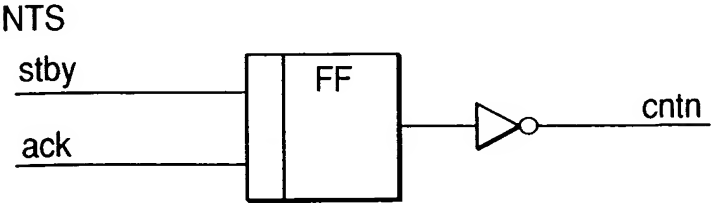


FIG. 7

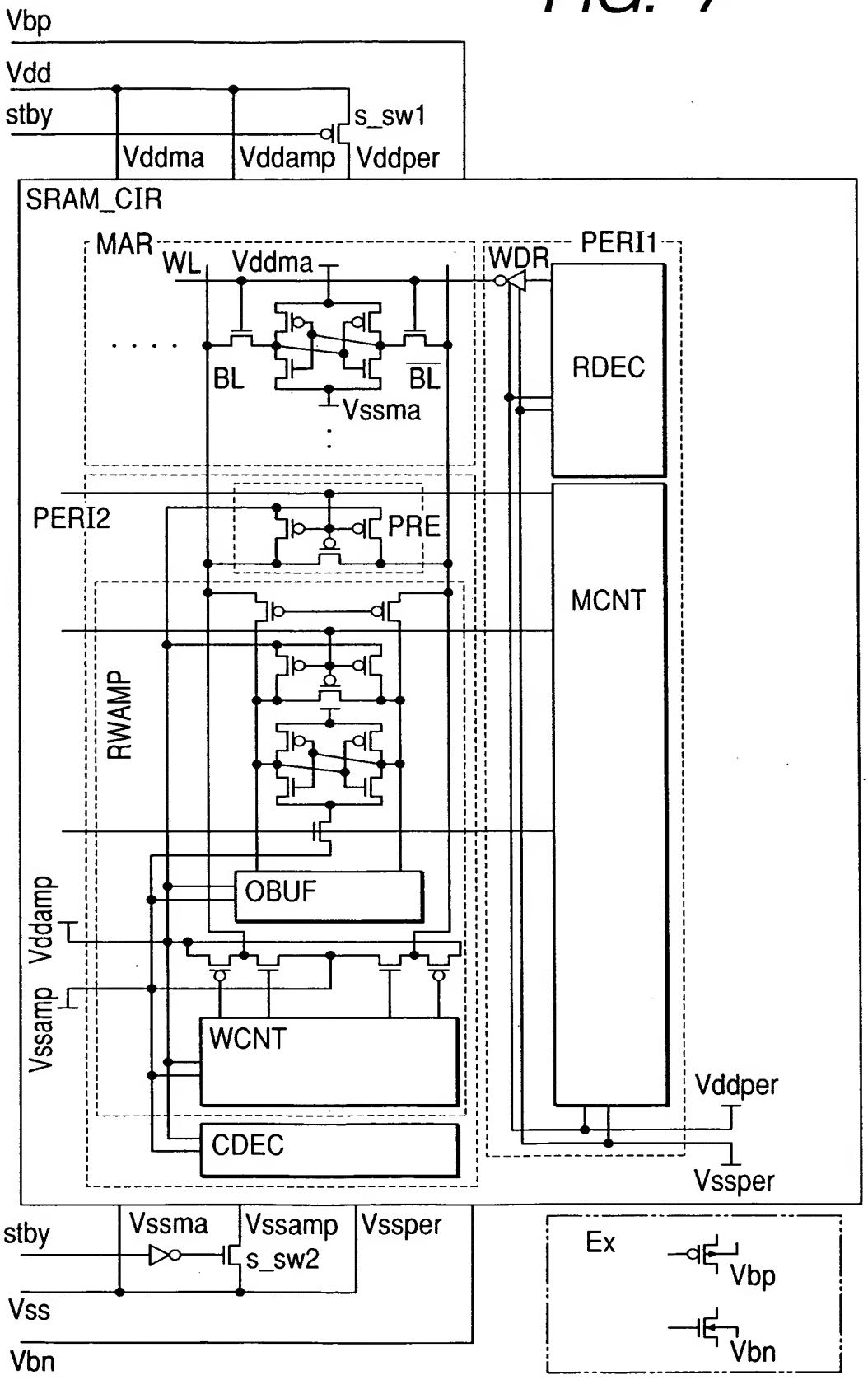

Vbp
Vdd
stby
s_sw1
Vddma
Vddamp
Vddper
SRAM_CIR
MAR
WL
Vddma
WDR
PERI1
BL
BL
Vssma
RDEC
PERI2
PRE
MCNT
RWAMP
OBUF
Vddamp
Vssamp
WCNT
CDEC
Vddper
Vssper
stby
Vssma
Vssamp
Vssper
s_sw2
Vss
Vbn
Ex
Vbp
Vbn

FIG. 8

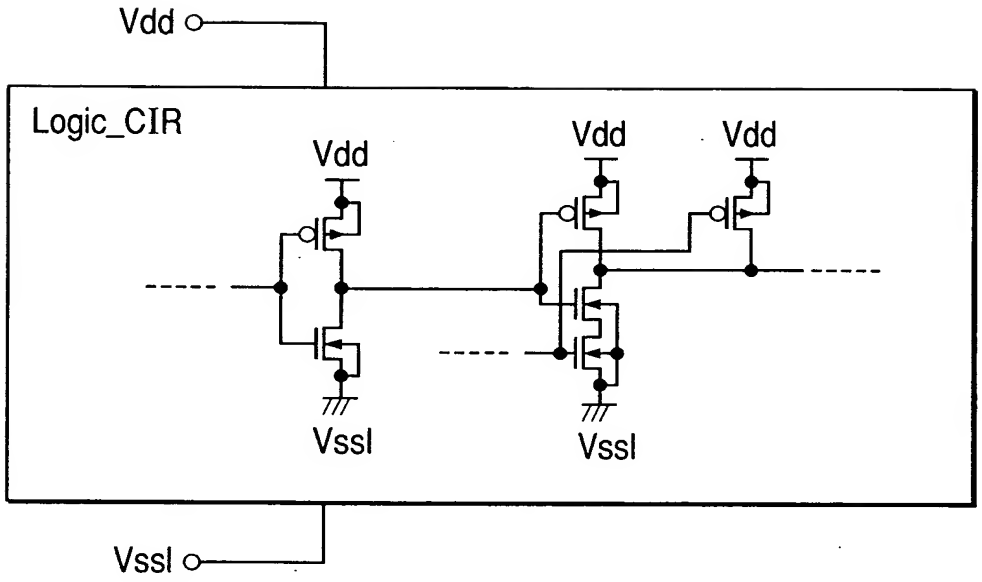


FIG. 9

		Logic_CIR	Logic sw (N1)	SRAM_CIR	SRAM sw (s_sw1, s_sw2)	IO
Pattern1	Tox Vth	2.0nm 0.25V, 0.40V	6.7nm 0.80V	2.0nm 0.25V, 0.40V	2.0nm 0.40V	6.7nm 0.80V
Pattern2	Tox Vth	2.0nm 0.25V, 0.40V	6.7nm 0.80V	2.0nm 0.25V, 0.40V	6.7nm 0.40V	6.7nm 0.80V
Pattern3	Tox Vth	2.0nm 0.25V, 0.40V	6.7nm 0.80V	2.0nm 0.25V, 0.40V	2.0nm 0.40V	6.7nm 0.80V

FIG. 10

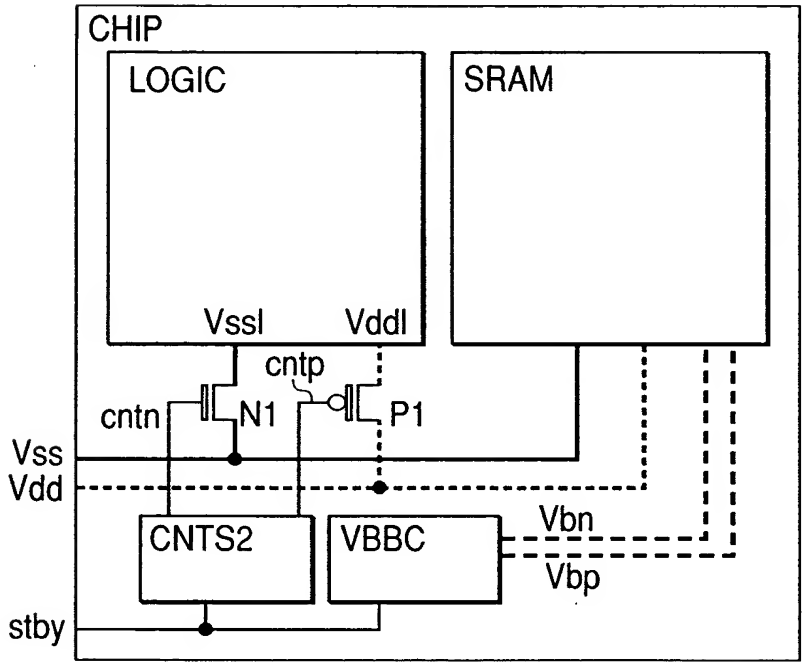

CHIP
LOGIC
SRAM
Vssl
Vddl
cntp
cntn
N1
P1
Vss
Vdd
CNTS2
VBBC
Vbn
Vbp
stby

FIG. 11

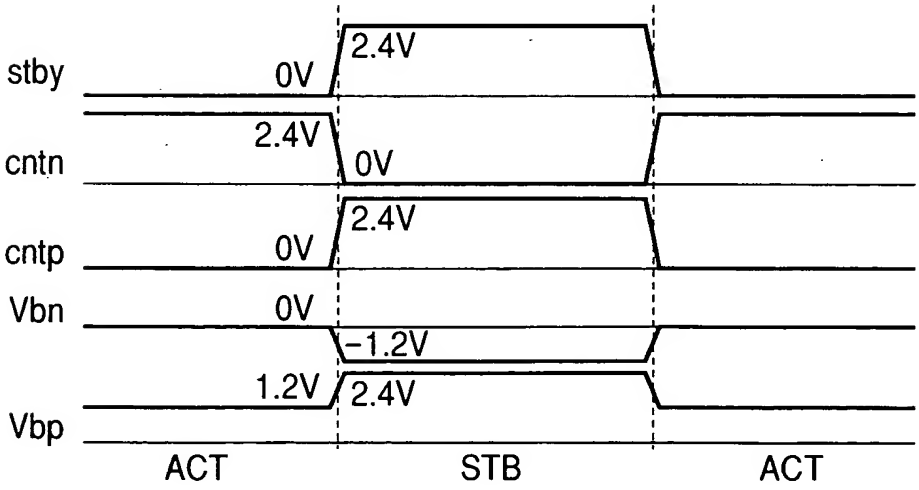

stby
0V
2.4V
cntn
2.4V
0V
cntp
0V
2.4V
Vbn
0V
-1.2V
Vbp
1.2V
2.4V
ACT
STB
ACT

FIG. 12

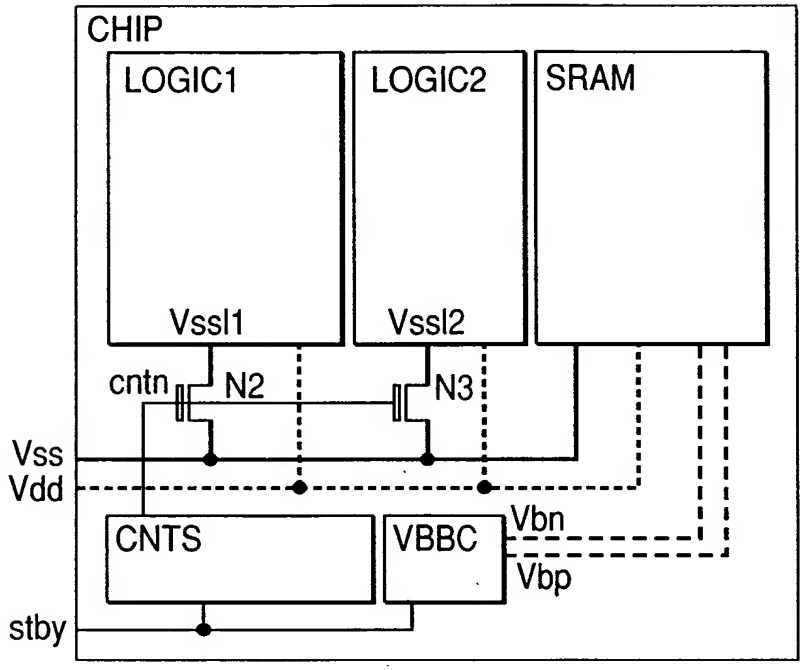

CHIP
LOGIC1
LOGIC2
SRAM
Vssl1
Vssl2
cntn
N2
N3
Vss
Vdd
CNTS
VBBC
Vbn
Vbp
stby

FIG. 13

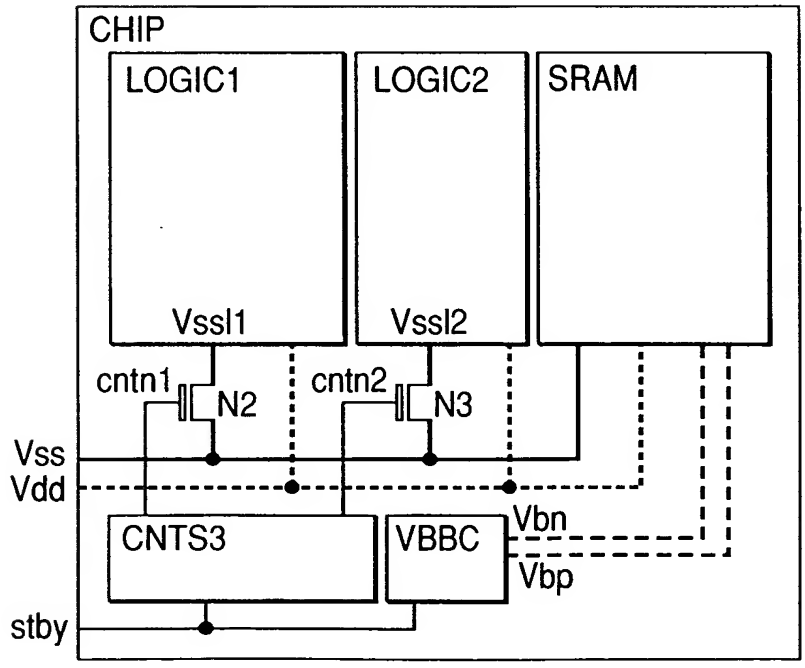

CHIP
LOGIC1
LOGIC2
SRAM
Vssl1
Vssl2
cntn1
N2
cntn2
N3
Vss
Vdd
CNTS3
VBBC
Vbn
Vbp
stby

FIG. 14

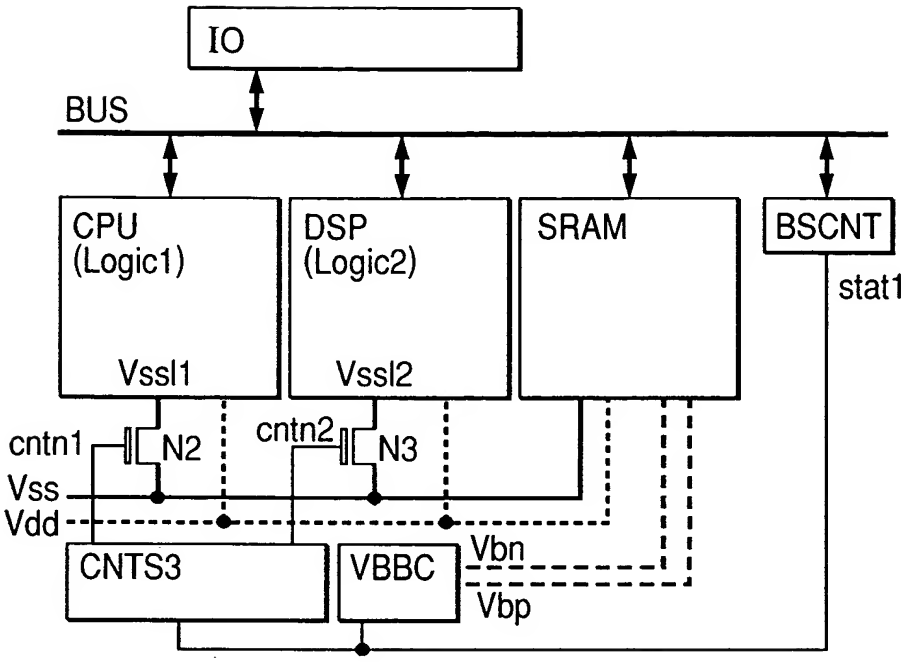

IO
BUS
CPU
(Logic1)
DSP
(Logic2)
SRAM
BSCNT
stat1
Vssl1
Vssl2
cntn1
N2
cntn2
N3
Vss
Vdd
CNTS3
VBBC
Vbn
Vbp

FIG. 15

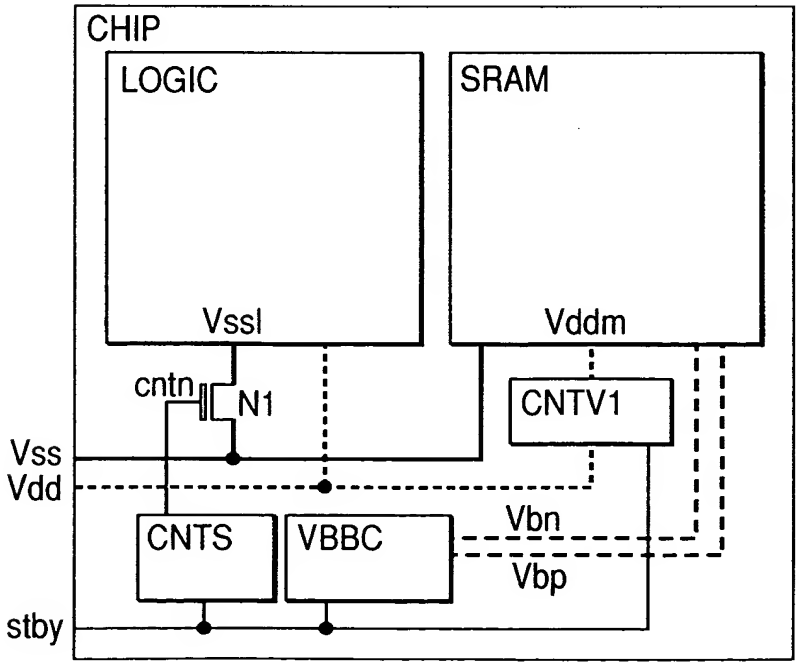

CHIP
LOGIC
SRAM
Vssl
Vddm
cntn
N1
CNTV1
Vss
Vdd
CNTS
VBBC
Vbn
Vbp
stby

FIG. 16

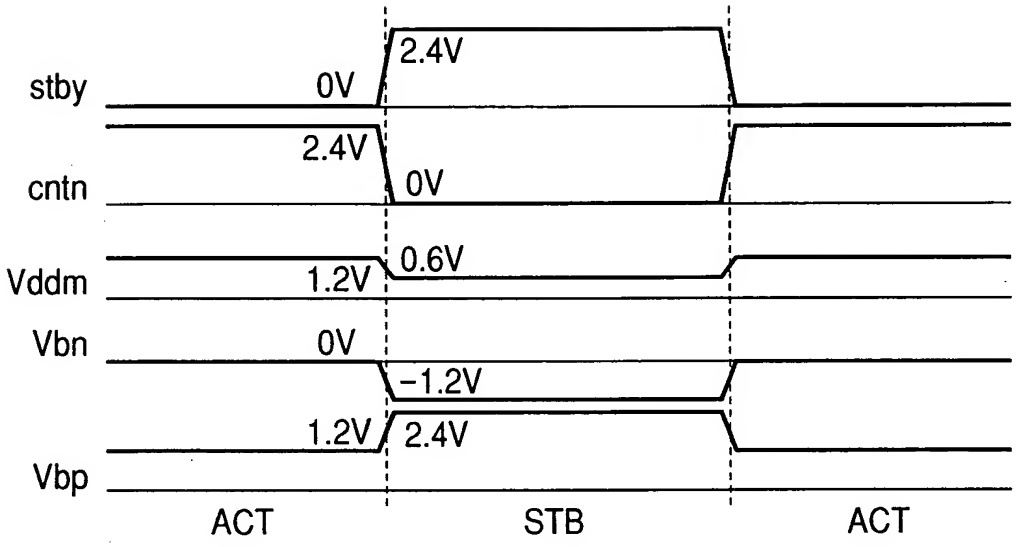

stby
0V
2.4V
cntn
2.4V
0V
Vddm
1.2V
0.6V
Vbn
0V
−1.2V
Vbp
1.2V
2.4V
ACT
STB
ACT

FIG. 17

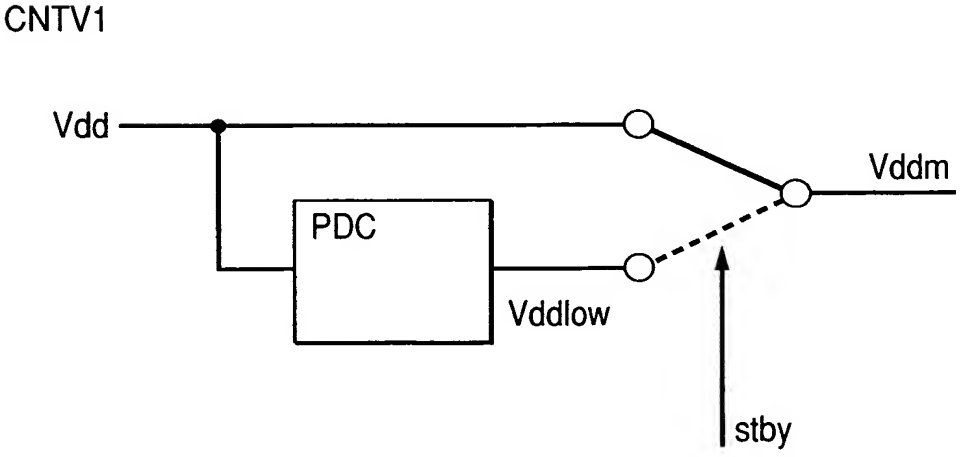

CNTV1
Vdd
PDC
Vddlow
Vddm
stby

FIG. 18

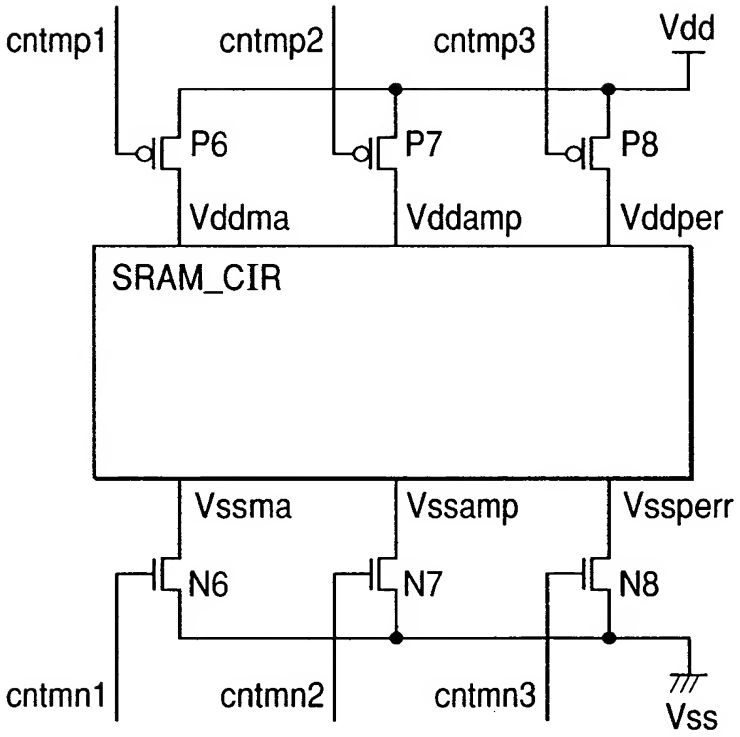

cntmp1
cntmp2
cntmp3
Vdd
P6
P7
P8
Vddma
Vddamp
Vddper
SRAM_CIR
Vssma
Vssamp
Vssperr
N6
N7
N8
cntmn1
cntmn2
cntmn3
Vss

FIG. 19

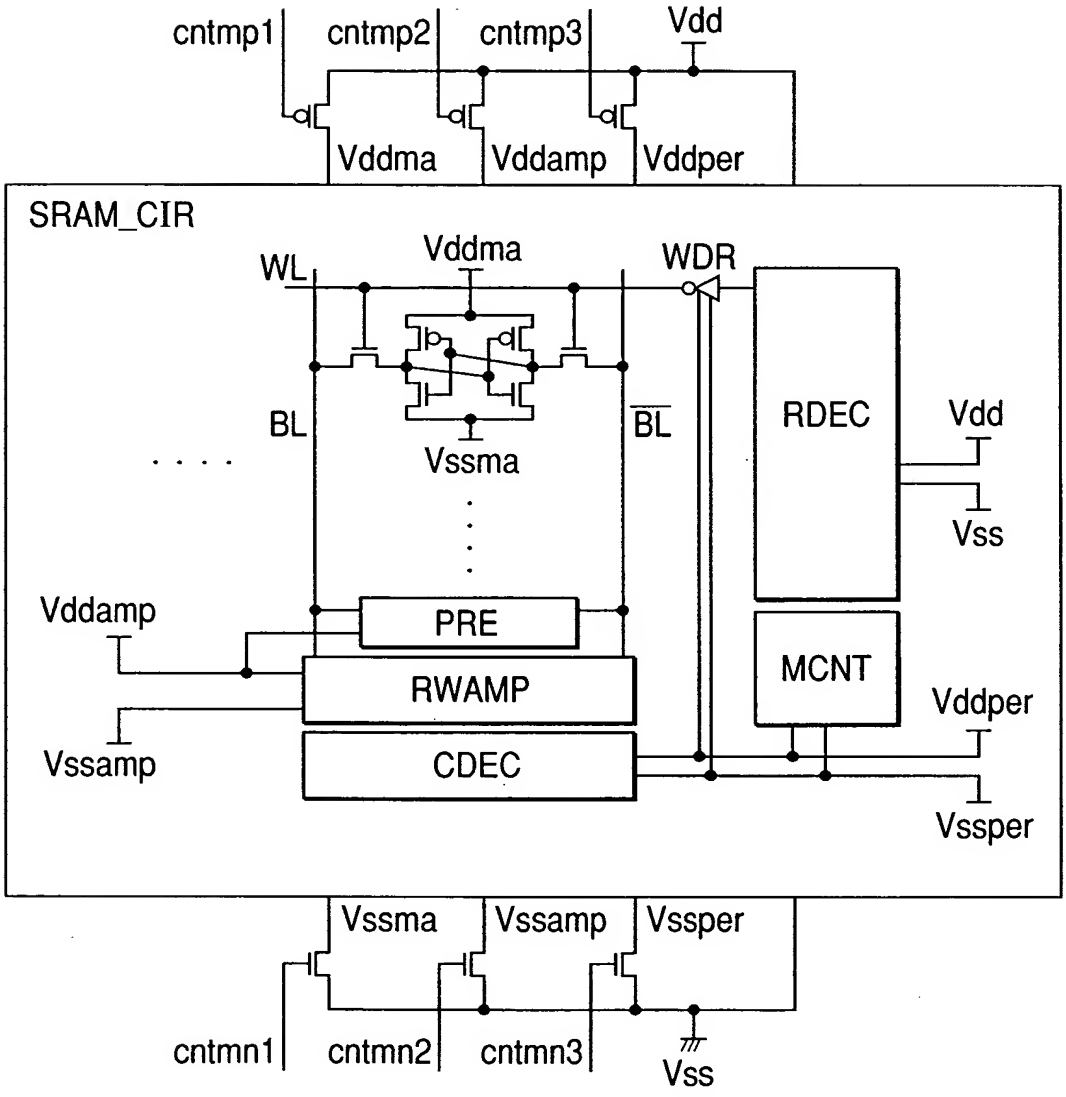

cntmp1
cntmp2
cntmp3
Vdd
Vddma
Vddamp
Vddper
SRAM_CIR
WL
Vddma
WDR
BL
Vssma
BL
RDEC
Vdd
Vss
Vddamp
PRE
RWAMP
MCNT
Vddper
Vssamp
CDEC
Vssper
Vssma
Vssamp
Vssper
cntmn1
cntmn2
cntmn3
Vss

FIG. 20

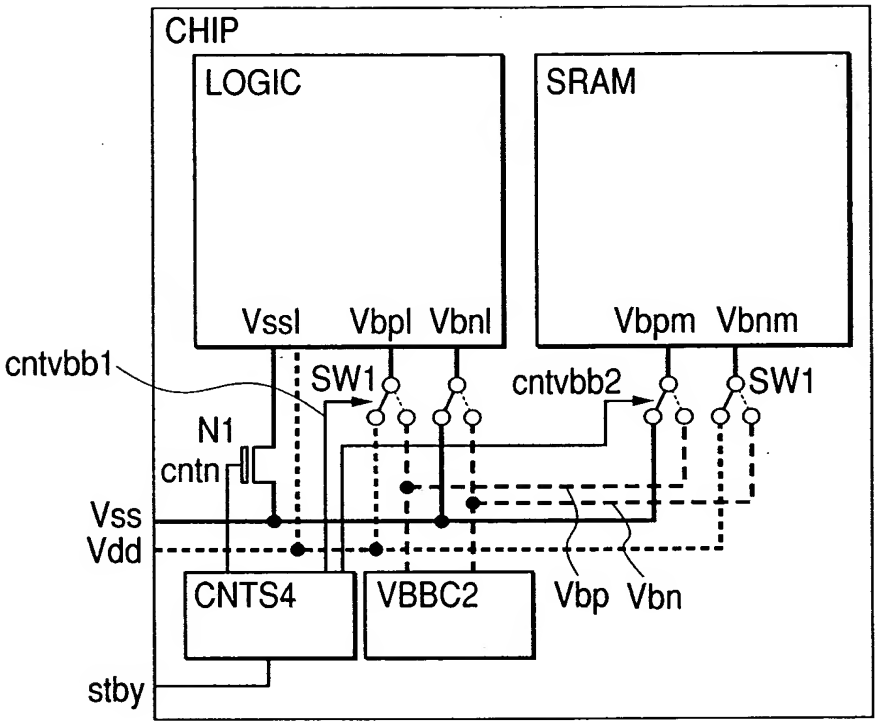

CHIP
LOGIC
SRAM
Vssl
Vbpl
Vbnl
Vbpm
Vbnm
cntvbb1
SW1
cntvbb2
SW1
N1
cntn
Vss
Vdd
CNTS4
VBBC2
Vbp
Vbn
stby

FIG. 21

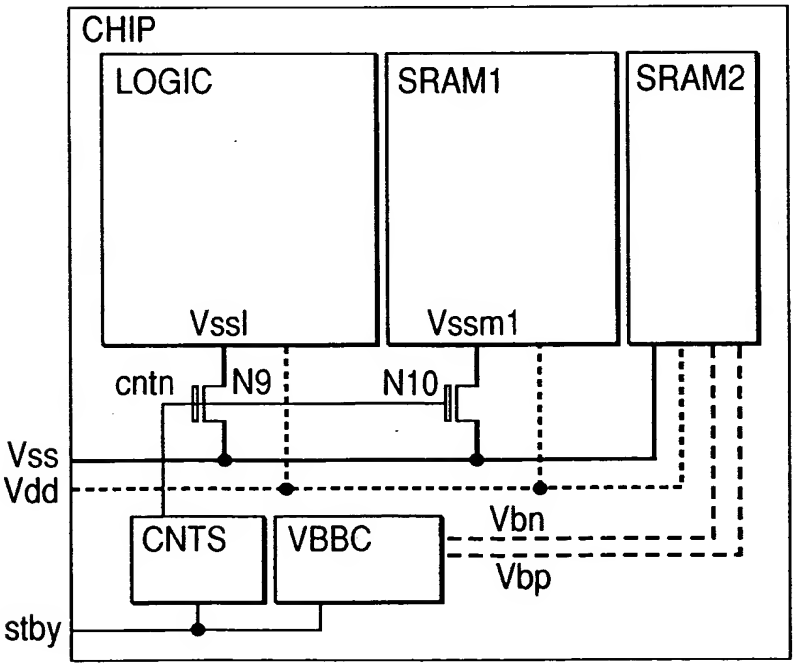

CHIP
LOGIC
SRAM1
SRAM2
Vssl
Vssm1
cntn
N9
N10
Vss
Vdd
CNTS
VBBC
Vbn
Vbp
stby

FIG. 22

		Logic_CIR	IO	MAR1	MAR2
Pattern1	Tox Vth	2.0nm 0.25V, 0.40V	6.7nm 0.80V	2.0nm 0.40V	2.0nm 0.40V
Pattern2	Tox Vth	2.0nm 0.25V, 0.40V	6.7nm 0.80V	2.0nm 0.40V	6.7nm 0.40V
Pattern3	Tox Vth	2.0nm 0.25V, 0.40V	6.7nm 0.80V	2.0nm 0.25V	2.0nm 0.40V
Pattern4	Tox Vth	2.0nm 0.25V, 0.40V	6.7nm 0.80V	2.0nm 0.25V	6.7nm 0.40V

FIG. 23

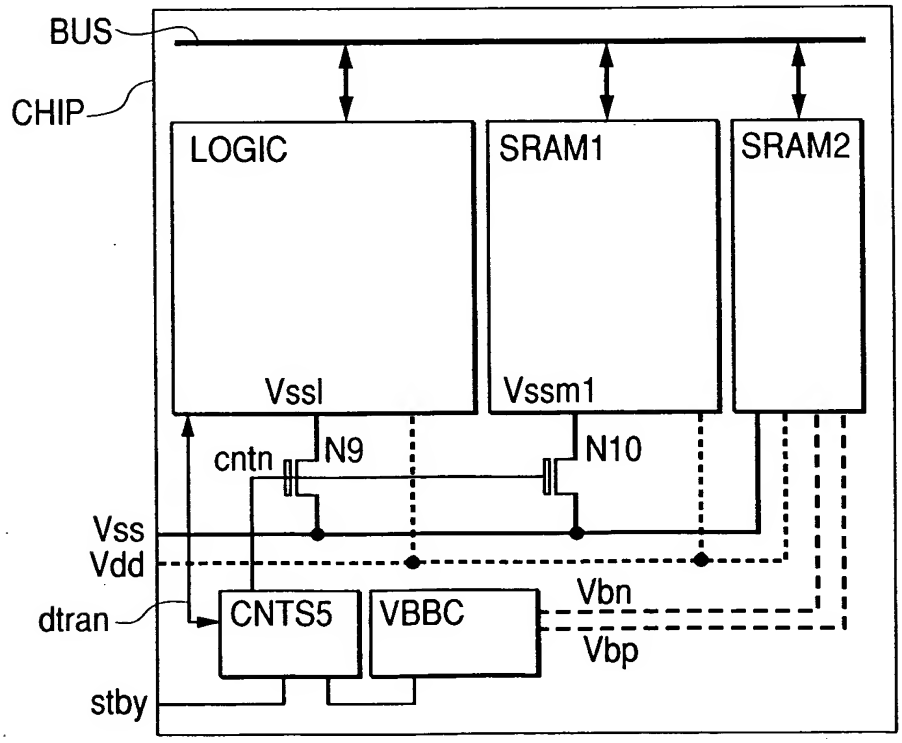


FIG. 24

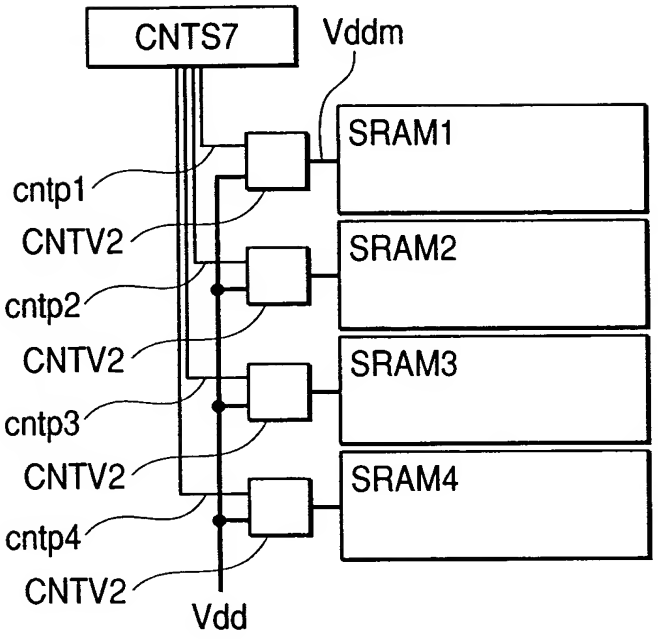
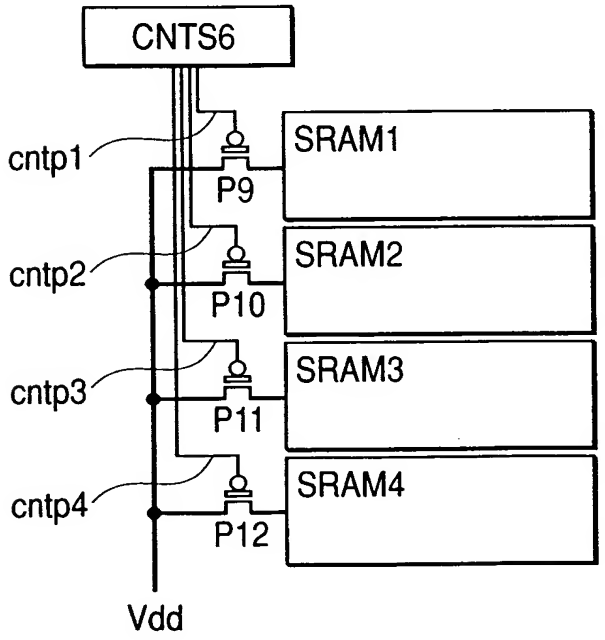

CNTS7
Vddm
SRAM1
SRAM2
SRAM3
SRAM4
cntp1
CNTV2
cntp2
CNTV2
cntp3
CNTV2
cntp4
CNTV2
Vdd

FIG. 25


CNTS6
SRAM1
SRAM2
SRAM3
SRAM4
cntp1
P9
cntp2
P10
cntp3
P11
cntp4
P12
Vdd

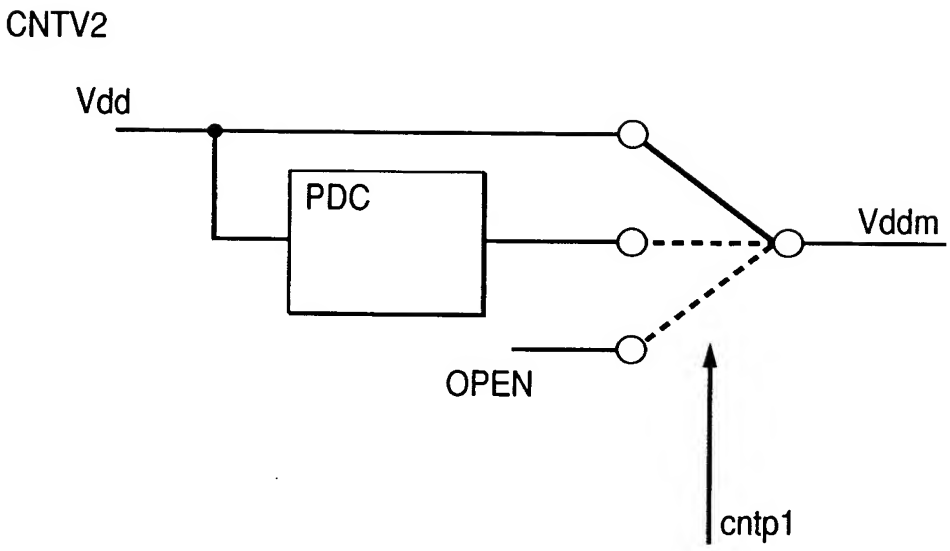



FIG. 26